10.6 Gbit/s 2:1 Time Division Multiplexer Using Dual Gate GaAs MESFETs

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Abstract

A 2:1 time division multiplexer (MUX) has been designed and built with dual gate GaAs MESFETs in thick film circuits. 10.6 Gbit/s NRZ pulses have been obtained. The voltage swing of MUX at 10 Gbit/s is 1V which is the largest one reported so far. The operation of MUX has been simulated by using mwSPICE and a good agreement between the measured and simulated switching waveforms has been obtained.

Introduction

When studying optical transmission bitrates above 5 Gbit/s, a time division multiplexer (MUX) becomes one of the key circuits in the system due to the lack of pulse word generators operating beyond 5 Gbit/s. Several MUXs operating above 10 Gbit/s have been reported. By using Si bipolar technology, a monolithically integrated MUX working at 11.4 Gbit/s has been obtained [1]. However, the design and fabrication of the circuit are relatively complicated. The use of hybrid integrated circuits (HICs) provides a simple way to build high speed circuits. An 11 Gbit/s MUX has been built with discrete HEMTs and HICs [2]. With discrete MESFET chips and HICs, 16 and 20 Gbit/s MUXs have been made [3-4]. However, the amplitudes of output voltage from the MUXs were rather small and not suitable for practical applications. Hence, an additional wide band and high gain amplifier must be applied to obtain large voltage swing for direct modulation of a semiconductor laser. Furthermore, no detailed design information and simulation results of the MUXs have been provided.

In this paper, we present design and test of a simple and flexible 2:1 MUX built with dual gate MESFETs and HICs. The maximum multiplexing output is 10.6 Gbit/s. At 10 Gbit/s, the output voltage swing of the MUX is 1V which is the largest one reported so far. The comparison between the measurement and simulation of the MUX is also shown.

Operation of MUX

The application of dual gate GaAs MESFETs in Gbit/s MUXs has already been demonstrated [5]. The circuit of the multi gigabits MUX used in the present work is shown in Fig.1. The NRZ pulse train and clock signal are applied to the first NAND gate. By adjusting time delay of the clock signal with respect to the data signal, RZ format pulses are obtained at the output of the NAND gate. A capacitor is used to provide DC isolation between the stages and the level shift of the output from the NAND gate. This simplifies circuit configuration of the MUX compared with the circuits of MUXs reported before. The RZ pulses are then divided by a wide band power splitter. The splitted signals are delayed with respect to each other before they are applied to the second NAND gate which is similar to the previous one. A phase shifter and two phase adjustable connectors have been used in different channels, respectively. This provides the flexibility of adjusting delay time for different input bitrates. The difference of the delay time between the two channels should be an odd number of half periods of input bitrate. This can easily be done by choosing the length of delay lines and adjusting the phase shifter and connectors. Theoretically, multiplexing can be performed for two input signals having a proper delay time difference. However, with increasing operating bitrate, large attenuation will result from the longer delay line and subsequently, amplitude fluctuation of the multiplexing output is produced. When the RZ signals with proper delay times are provided, NRZ pulses with double bitrates are obtained at the output of the second NAND gate.

Design of MUX

The circuit diagram of the NAND gate is shown in Fig.2. The dual gate MESFETs used are of the type NE25000 with f_{max} 60GHz. They have been bonded with gold wire of diameter 0.025 mm in a thick film circuit. The thickness of the substrate used is 0.635 mm and dielectric constant is 9.3.

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The input matching resistors R_{g1} and R_{g2} are trimmed to 50 Ω and the biasing resistor R_d is chosen to be 100 Ω. By using thick film technology, the cost of fabrication is greatly reduced. The coupling capacitor is simply a bias network (HP-11612A) with bandwidth of 45MHz-26.5GHz. The power divider is a resistive one with typical bandwidth of DC-26GHz and insertion loss of 6dB. The phase shifter is a precision coaxial one with variable phase shift for the full frequency range of DC-26GHz. The phase adjustable connectors with bandwidth of DC-26GHz are the combination of connector and phase shifter that allow phase adjustment and trimming to be performed during the test of MUX.

Test and Simulation of MUX

The MUX has been built and tested. The 2^7-1 pseudorandom NRZ data and clock signal are produced by a 5Gbit/s Anritsu word generator with rise and fall times about 70ps, respectively. The multiplexed output is displaced on an HP 54128 sampling oscilloscope with rise time of 20ps. After passing through the pulse converter, coupling capacitor, and power divider, the RZ pulses have been attenuated by 6dB, and the peak-to-peak value of the voltage swing is about 1.2V as shown in Fig.3. It can be seen that the high and low levels of the pulses are 0.4V and -0.8V, respectively. Such levels are compatible with the required input levels of the next NAND gate. The multiplexing test has been performed at bitrate above 5 Gbit/s. The eye diagram of 6 Gbit/s and 10 Gbit/s are shown in Fig.4 and Fig.5, respectively. It can be seen that a clearer and more open eye diagram has been obtained at 6 Gbit/s compared with that at 10 Gbit/s. At 10 Gbit/s, the eye diagram is still sufficiently open for the bit pattern to be useful. The measured rise and fall times are 35ps and 40ps, respectively. The peak-to-peak voltage swing is 1V. This is the largest voltage swing reported so far at 10 Gbit/s. By using an external clock signal of 5.3 GHz, the pulse generator can work at 5.3 Gbit/s and thus the MUX performs multiplexing at 10.6 Gbit/s. The waveforms of the 10.6 Gbit/s pulses are shown in Fig.6. The MUX has been simulated by using mwSPICE. The model of dual gate MESFETs is simply two single gate MESFETs in series connection [6]. The model parameters are estimated based on data sheet and published literatures. The measured and simulated waveforms for 5 Gbit/s RZ and 10 Gbit/s NRZ pulses are shown in Fig.7 and Fig.8, respectively. It can be seen that the agreement between the measured and simulated waveforms is good.

Conclusion

A 2:1 MUX operating up to 10.6Gbit/s NRZ output has been demonstrated in this paper. The MUX is simple, flexible and of low cost. At 10 Gbit/s, the largest reported voltage swing of 1V has been obtained. The operation of the MUX has been verified by mwSPICE and a good agreement between the measured and simulated results has been obtained.

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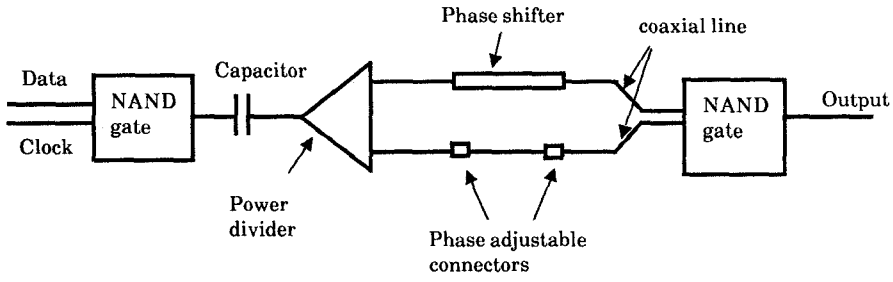


Fig.1 Circuit of 2:1 time division multiplexer circuit

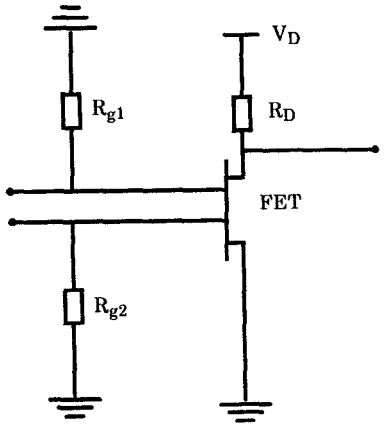


Fig.2 Circuit of NAND gate

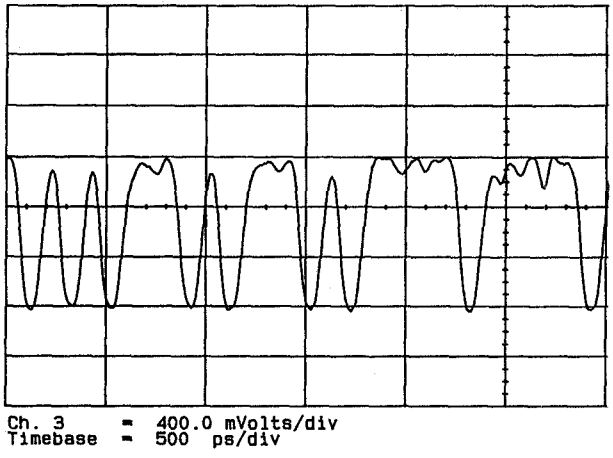
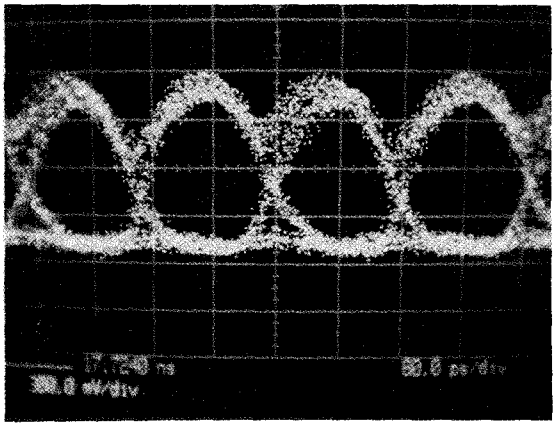
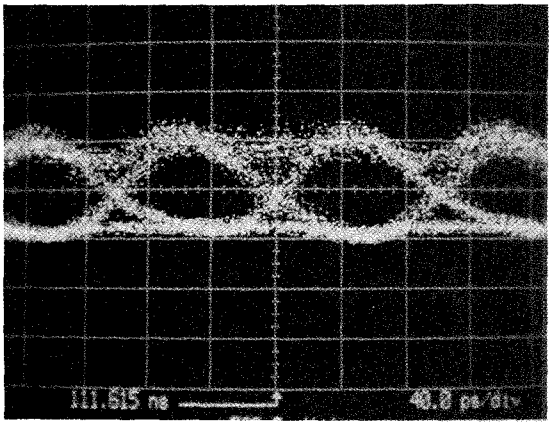


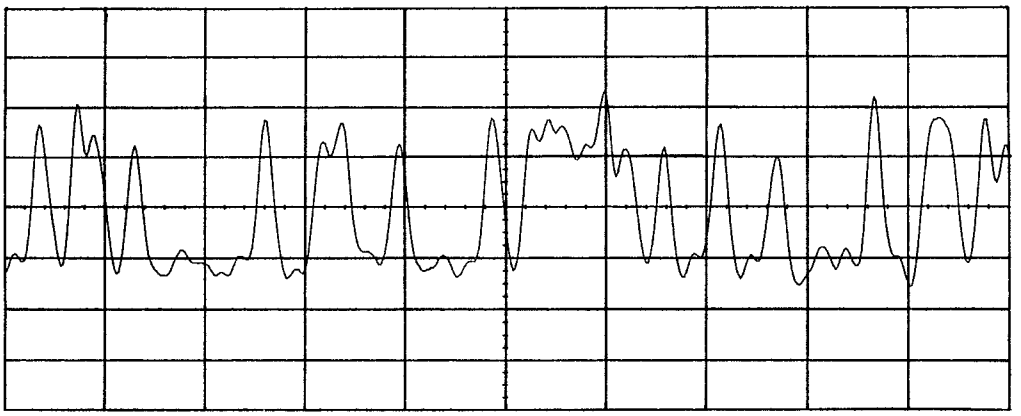
Fig.3 5 Gbit/s RZ data stream after power splitter



H: 80ps/div V: 300mv/div
Fig.4 6 Gbit/s eye diagram

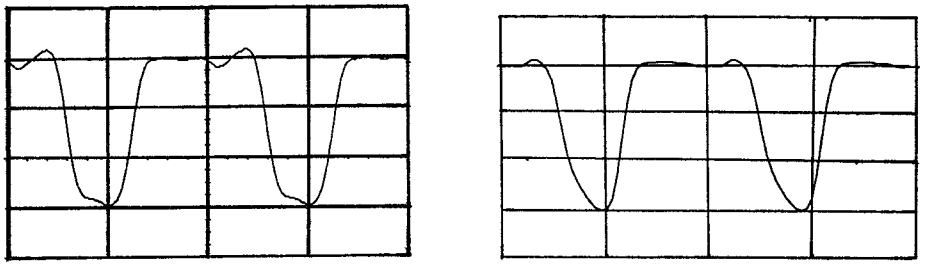


H: 40ps/div V: 500mv/div
Fig.5 10 Gbit/s eye diagram



H: 500ps/div V: 200mv/div

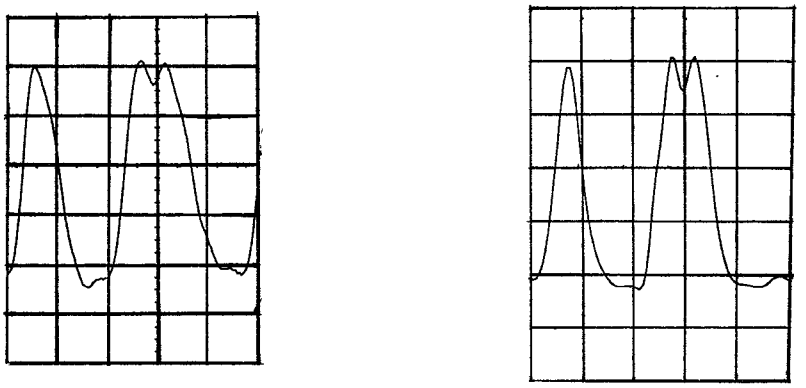
Fig.6 Waveforms of MUX at 10.6Gbit/s



(a) Measured waveforms (b) Simulated waveforms

H: 200ps/div V:500mv/div

Fig.7 Comparision of measured and simulated 5 Gbit/s RZ pulses



1001100 1001100

(a) Measured waveforms (b) Simulated waveforms

H: 150ps/div V: 300mv/div

Fig.8 Comparision of measured and simulated 10 Gbit/s NRZ pulses